REMARKS

This Amendment is in response to the Office Action dated April 13, 2005. Applicant respectfully requests reconsideration and allowance of all pending claims in view of the above-amendments and the following remarks.

In addition, Applicant would like to thank the Examiner for the indication of allowable subject matter in claims 2, 12, 14 and 20.

I. CLAIM OBJECTIONS AND REJECTIONS UNDER §112

Claims 1, 3, 5, 12, 15, 16, 17 and 19 were objected to because of minor informalities in the claims. In addition, claims 1-20 were rejected under §112, second paragraph, as being indefinite.

Accordingly, the claims are amended in order to meet the claim objections and the rejections under §112. The following are explanations concerning Applicant's amendments related to the Examiner's formal objections:

Concerning claim 1:

- "means of delivering to at least one output a predetermined output voltage representative of a logic level" correspond to the circuit of figure 4;
- "means of distributing a mains voltage" have been replaced by "means of generating a main voltage";
- "means of generating an internal reference voltage lower than the main voltage" correspond to TP2 on figure 4;
- "means of connecting the main voltage on the output" correspond to reference number 31 on figure 4;

- "means of limiting and/or detecting the voltage on the output at the value of the predetermined output voltage" correspond to reference number 32 on figure 4.

Concerning claims 3 and 7:

- "means of connecting the main voltage" have been replaced by "connecting means" which correspond to "means of connecting the main voltage on the output" of claim 1;
- concerning the fact that the currents (and not the voltage as believed by the Examiner) circulating in the connecting means and in the limiting and/or detecting means are balanced, this characteristic is explained in page 11, lines 12-20 of the present application.

Concerning claim 12:

As explained page 11, lines 9-11, "the transistor TP5 (which is comprised by the second mirror) is configured in such a way that it is able to impose its level on transistor TN3 (fourth transistor) the latter being a very weak transistor". According to the Examiner, claim 12 as filed comprises a mistake, which we corrected by replacing "third transistor" by "fourth transistor".

Concerning claim 16:

Claim 16 has approximately the same scope as claim 1, consequently we modified claim 16 in the same way that we modified claim 1. The explanation given above concerning claim 1 can be applied to claim 16.

Concerning claim 18 and 19:

The first power transistor and the primary transistor are the same transistor. Consequently, claims have been modified in order to replace "primary transistor" by "first transistor".

II. CLAIM REJECTIONS

Claims 1, 3-11, 13 and 16-19 are rejected under §102(b) as being anticipated by Sukegawa et al., U.S. Patent No. 6,169,698. However, the Examiner indicated that claims 2, 12, 14 and 20 would be allowable if rewritten to overcome the rejections under §112, second paragraph.

Accordingly, in the new set of claims:

- Amended claim 1 is a combination of original claims 1 and 2;
- New claim 21 is a combination of original claims 1, 4, 8, 9, 10, 11 and 12;
- New claim 22 is a combination of original claims 1 and 14;
- New claim 23 is a combination of original claims 1 and 20;
- Original claims 2, 17, 18, 19 and 20 have been deleted.

Since the Office Action indicated that claims 2, 12, 14 and 20 (now included in claims 1, 16 and 21-23) would be allowable, these new claims should therefore be in condition for allowance.

Consideration and allowance of all pending claims are respectfully requested.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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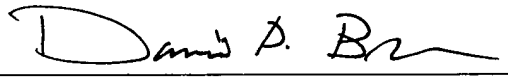
By: 

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